M5M418165BJ,TP-6,-7,-8,-6S,-7S,-8S

HYPER PAGE MODE 16777216-BIT (1048576-WORD BY 16-BIT) DYNAMIC RAM

DESCRIPTION

This is a family of 1048576-word by 16-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation , and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

Type name	$\overline{RAS}$ access time (max.ns)	$\overline{CAS}$ access time (max.ns)	Address access time (max.ns)	$\overline{OE}$ access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M418165BXX-6,6S	60	15	30	15	110	850
M5M418165BXX-7,7S	70	20	35	20	130	750
M5M418165BXX-8,8S	80	20	40	20	150	650

XX=J,TP

- Standard 42 pin SOJ,50 pin TSOP
- Single 5.5V ±10% supply
- Low stand-by power dissipation
  5.5mW (Max) ····· CMOS input level
- Low operating power dissipation
  M5M418165Bxx- 6,6S ---------- 940.0mW (Max)
  M5M418165Bxx- 7,7S ---------- 830.0mW (Max)
  M5M418165Bxx- 8,8S ---------- 720.0mW (Max)

- Hyper-page mode , Read-modify-write, $\overline{RAS}$-only refresh
  $\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh capabilities
- Early-write mode and $\overline{OE}$ to control output buffer impedance
  All inputs, output TTL compatible and low capacitance
- 1024 refresh cycles every 16.4ms (A_0 ~A_9)

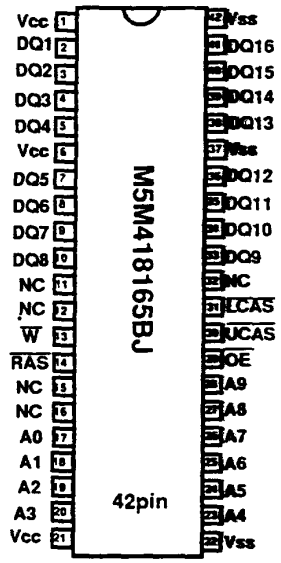
APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

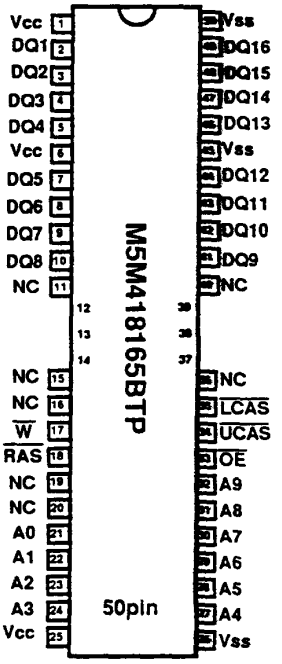
PIN DESCRIPTION

Pin Name	Function
A_0-A_9	Address Inputs
DQ_1-DQ_{16}	Data Inputs / Outputs
$\overline{RAS}$	Row Address Strobe Input
$\overline{UCAS}$	Upper Bite Control Column Address Strobe Input
$\overline{LCAS}$	Lower Bite Control Column Address Strobe Input
$\overline{W}$	Write Control Input
$\overline{OE}$	Output Enable Input
Vcc	Power Supply (+5.0V)
Vss	Ground (0V)

PIN CONFIGURATION (TOP VIEW)



Outline 42P0K (400mil SOJ)



Outline 50P3W-L (400mil TSOP Normal Bend)

FUNCTION

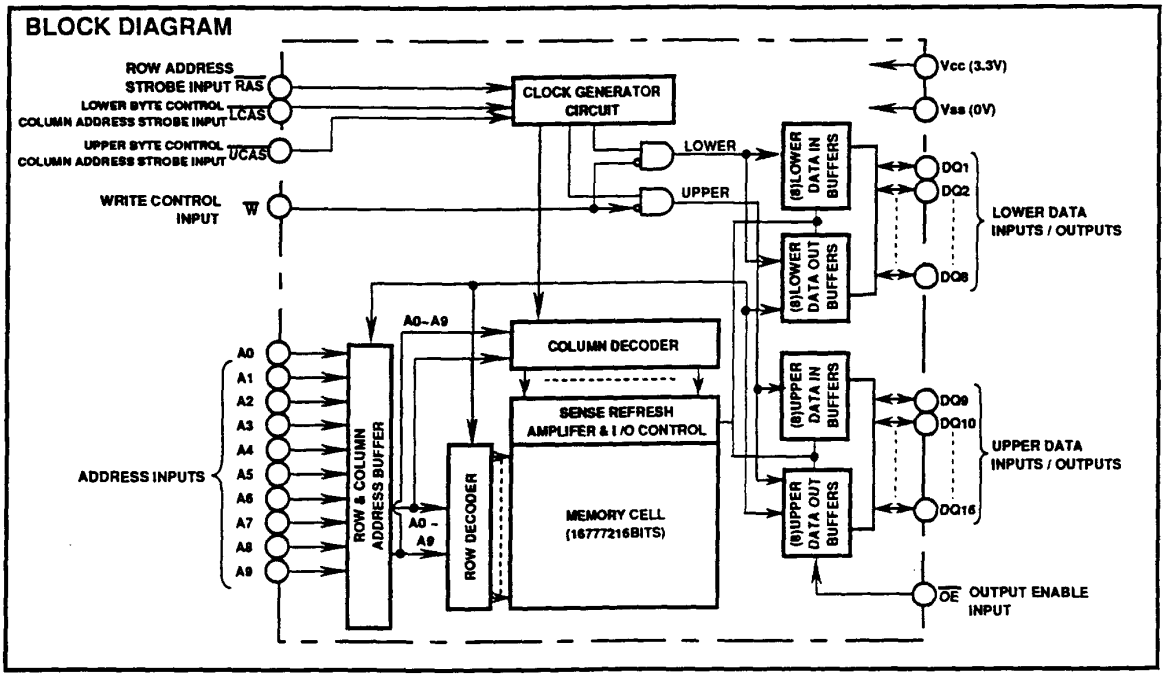
The M5M418165BJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., hyper page mode, $\overline{RAS}$ only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output	
	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{OE}$	DQ1-DQ8	DQ9-DQ16
Lower byte Read	ACT	ACT	NAC	NAC	ACT	DOUT	OPN
Upper byte Read	ACT	NAC	ACT	NAC	ACT	OPN	DOUT
Word Read	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
Lower Byte Write	ACT	ACT	NAC	ACT	NAC	DIN	DNC
Upper Byte Write	ACT	NAC	ACT	ACT	NAC	DNC	DIN
Word write	ACT	ACT	ACT	ACT	NAC	DIN	DIN
$\overline{RAS}$-only refresh	ACT	NAC	NAC	DNC	DNC	OPN	OPN
Hidden refresh	ACT	ACT	ACT	NAC	ACT	DOUT	DOUT
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	ACT	DNC	DNC	OPN	OPN
Standby	NAC	DNC	DNC	DNC	DNC	OPN	OPN

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid,APD : applied, OPN : open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to Vss	-1~7	V
VI	Input voltage		-1~7	V
VO	Output voltage		-1~7	V
IO	Output current		50	mA
Pd	Power dissipation	Ta=25°C	1000	mW
Topr	Operating temperature		0~70	°C
Tstg	Storage temperature		-65~150	°C

RECOMMENDED OPERATING CONDITIONS (Ta=0~70°C, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5.0	5.5	V
Vss	Supply voltage	0	0	0	V
V_{IH}	High-level input voltage, all inputs	2.4		6.0	V
V_{IL}	Low-level input voltage, all inputs	-1		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta=0~70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		I_{OH}=-5.0mA	2.4		Vcc	V
V_{OL}	Low-level output voltage		I_{OL}=4.2mA	0		0.4	V
I_{OZ}	Off-state output current		Q floating 0V≤V_{OUT}≤5.5V	-5		5	μA
I_I	Input current		0V≤V_{IN}≤6V, Other inputs pins=0V	-5		5	μA
I_{CC1} (AV)	Average supply current from Vcc operating (Note 3,4,5)	M5M418165B-6,6S	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC}=t_{WC}=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	
I_{CC2}	Supply current from Vcc, stand-by (Note 6)		$\overline{RAS}$=$\overline{CAS}$=V_{IH} output open			2	mA
			$\overline{RAS}$=$\overline{CAS}$≥Vcc-0.2 V			1	
I_{CC3} (AV)	Average supply current from Vcc refreshing (Note 3,5)	M5M418165B-6,6S	$\overline{RAS}$ cycling, $\overline{CAS}$=V_{IH} t_{RC}=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	
I_{CC4}(AV)	Average supply current from Vcc Hyper-Page-Mode (Note 3,4,5)	M5M418165B-6,6S	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ cycling t_{PC}=min. output open			135	mA
		M5M418165B-7,7S				115	
		M5M418165B-8,8S				95	
I_{CC5}(AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M418165B-6,6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC}=min. output open			170	mA
		M5M418165B-7,7S				150	
		M5M418165B-8,8S				130	

Note 2: Current flowing into an IC is positive, out is negative.

3: Icc1 (AV), Icc3 (AV) and Icc4 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.

4: Icc1 (AV) and Icc4 (AV) are dependent on output loading. Specified values are obtained with the output open.

5: Column Address can be changed once or less while RAS=V_{IL} and $\overline{LCAS}$/$\overline{UCAS}$=V_{IH}.

CAPACITANCE (Ta=0 ~ 70°C, Vcc=5.0V ±10%, Vss=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	M5M418165BJ, TP	V_I=Vss f=1MHz V_I=25mVrms			5	pF
$C_{I(\overline{OE})}$	Input capacitance, $\overline{OE}$ input					7	pF
$C_{I(\overline{W})}$	Input capacitance, write control input					7	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input					7	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input					7	pF
$C_{I/O}$	Input/Output capacitance, data ports					8	pF

SWITCHING CHARACTERISTICS (Ta=0 ~ 70°C, Vcc = 5V ±10%, Vss=0V, unless otherwise noted , see notes 6,14,15)

Symbol	Parameter		Limits						Unit
			M5M418165B-6,6S		M5M418165B-7,7S		M5M418165B-8,8S		
			Min	Max	Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 7,8)		15		20		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 7,9)		60		70		80	ns
tAA	Column address access time	(Note 7,10)		30		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 7,11)		35		40		45	ns
tOEA	Access time from $\overline{OE}$	(Note 7)		15		20		20	ns
tOHC	Output hold time from $\overline{CAS}$		5		5		5		ns
tOHR	Output hold time from $\overline{RAS}$	(Note 13)	5		5		5		ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 7)	5		5		5		ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 12)		15		20		20	ns
tWEZ	Output disable time after $\overline{WE}$ high	(Note 12)		15		20		20	ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 12,13)		15		20		20	ns
tREZ	Output disable time after $\overline{RAS}$ high	(Note 12,13)		15		20		20	ns

Note 6: An initial pause of 500 μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause . And any 8 $\overline{RAS}$ or $\overline{RAS}$/$\overline{CAS}$ cycles are required after prolonged periods (greater than 64 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

7: Measured with a load circuit equivalent to VOH=2.4V(IOH=-5mA) / VOL=0.4V(IOL=-4.2mA) load 100pF.

8: Assumes that $t_{RCD} \geq t_{RCD(max)}$ and $t_{ASC} \geq t_{ASC(max)}$ and $t_{CP} \geq t_{CP(max)}$.

9: Assumes that $t_{RCD} \leq t_{RCD(max)}$ and $t_{RAD} \leq t_{RAD(max)}$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by amount that t_{RCD} exceeds the value shown.

10: Assumes that $t_{RAD} \geq t_{RAD(max)}$ and $t_{ASC} \leq t_{ASC(max)}$.

11: Assumes that $t_{CP} \leq t_{CP(max)}$ and $t_{ASC} \geq t_{ASC(max)}$.

12: $t_{OEZ\,(max)}$,$t_{WEZ(max)}$,$t_{OFF(max)}$ and $t_{REZ(max)}$defines the time at which the output achieves the high impedance state ($I_{OUT} \leq$ ±10 uA) and is not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

13: Output is disabled after both $\overline{RAS}$ and $\overline{CAS}$ go to high.